Q4. 56

Q5.

// assume inputs are X0, X1 and return through X6

SUB SP,SP,0x18

STUR LR,[SP,0x10]

STUR X1,[SP,0x8] // b

STUR X0,[SP,0x0] // a // store the inputs and SP

ADD X5, XZR, XZR // z

BL average

LDUR LR,[SP,0x10]

LDUR X1,[SP,0x8] // b

LDUR X0,[SP,0x0] // a // restore the inputs and SP

SUBS XZR, x0, x5 // X5 does not need to be restored because it was not modified

B.GE Else

ADD X6, X1, #4 // crating b+4

ADD SP,SP,0x18 // pop three items off the stack and return b+4

BR LR

average:

SUB SP, SP, 0x18

STUR LR, [SP, 0x10]

STUR X1, [SP, 0x8] // b

STUR X0, [SP, 0x0] // a

ADD X6, XZR, XZR // y

ADD X7, X1, X0 // a + b

LSR X7, X7, #1 // divided by 2

ADD X6, XZR, X7

SUBS XZR, X6, # 0

B.G else

ADD SP, SP, 0x18 // pop three items off the stack and return y

BR LR

else:

ADD X6, XZR, #1

ADD SP, SP, 0x18 // pop three items off the stack and return 1

BR LR // return to caller

Else:

ADD X6, X0, #2 // creating a+2

ADD SP, SP, 0x18 // pop three items off the stack and return a+2

BR LR // return to the caller

Q6.

0xb500F183 =0b10110101000000001111000110000011

1. 10110101 indicates CBNZ
2. Given in the instruction, the hex value of COND\_BR\_address is 0b0000000011110001100 = 0x78C
3. We see the COND\_BR\_address is 0000000011110001100 in the instruction, but we have to add two zeros at the back which becomes 0b000000001111000110000 = 0x1E30
4. Address of the branch target: 0x78C

Q8

1. 0x5D00000000
2. 0x2A000000

Q10.

Answer 6: text

I am pretty sure the answer is text, and I got only got partial credit because my answer was not exact match. Please double check for me.

Q11.

1. 0x5000
2. 0x8
3. 0x2048 (where the BR LR instruction locates)

Q12. SUB X2, X7, 0x804

SUB is I type instruction,

Opcode ALU\_immediate Rn Rd

31 – 22 21 -10 9 – 5 4- 0

SUB 0x804 X7 X2

11001011000 100000000100 00111 00011

Thus the answer is 110010110001000000001000011100011